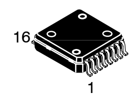
Freescale Semiconductor
Technical Data

Document Number: MHV5IC1810N
Rev. 0, 5/2006

RF LDMOS Wideband Integrated Power Amplifier

MHV5IC1810NR2

1805-1990 MHz, 5 W AVG., 28 V GSM/GSM EDGE RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIER



CASE 978-03
PFP-16
PLASTIC

The MHV5IC1810N wideband integrated circuit is designed with on-chip matching that makes it usable from 1805 to 1990 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulation formats.

Final Application

- Typical Two-Tone Performance: V_{DD} = 28 Volts, I_{DQ1} = 120 mA, I_{DQ2} = 90 mA, P_{out} = 5 Watts Avg., Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)
  Power Gain — 29 dB
  Power Added Efficiency — 29%
  IMD — -34 dBc

Driver Application

- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ1} = 105 mA, I_{DQ2} = 95 mA, P_{out} = 35 dBm, Full Frequency Band (1805-1880 MHz or 1930-1990 MHz)
  Power Gain — 29 dB
  Spectral Regrowth @ 400 kHz Offset = -67 dBc
  Spectral Regrowth @ 600 kHz Offset = -76 dBc
  EVM — 1.1% rms
- Capable of Handling 3:1 VSWR, @ 28 Vdc, 1990 MHz, 10 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 10 W CW P_{out}.

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, >5 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- RoHS Compliant
- In Tape and Reel. R2 Suffix = 1500 Units per 16 mm, 13 inch Reel.

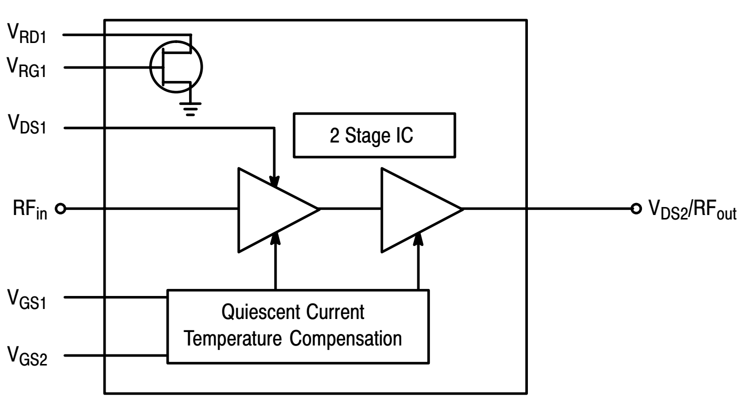
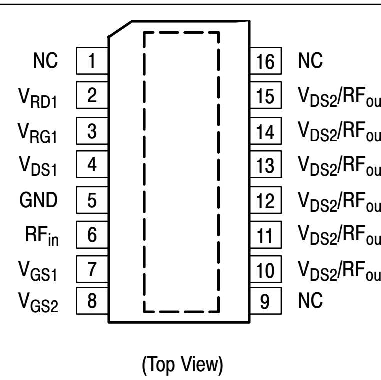


Figure 1. Functional Block Diagram



Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +12	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	150	°C
Input Power	P_{in}	12	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Final Application (P_{out} = 10 W CW)	Stage 1, 28 Vdc, I_{DQ1} = 120 mA		9.2	
	Stage 2, 28 Vdc, I_{DQ2} = 90 mA		3.3	
Driver Application (P_{out} = 2.25 W CW)	Stage 1, 28 Vdc, I_{DQ1} = 120 mA		10	
	Stage 2, 28 Vdc, I_{DQ2} = 90 mA		3.5	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

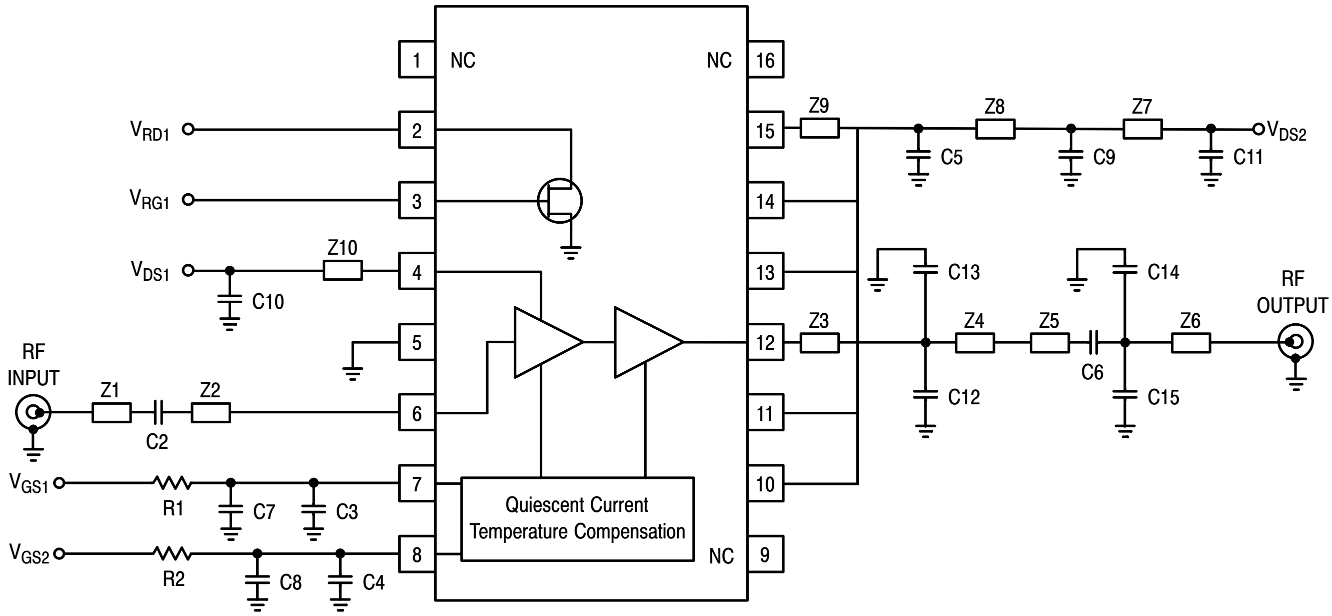
Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Wideband 1930-1990 MHz Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 120 mA, I_{DQ2} = 90 mA, P_{out} = 5 W Avg., f1 = 1990 MHz, f2 = 1990.1 MHz, Two-Tone Test					
Power Gain	G_{ps}	26.5	29	—	dB
Power Added Efficiency	PAE	25	29	—	%
Intermodulation Distortion	IMD	—	-34	-27	dBc
Input Return Loss	IRL	—		-10	dB
Typical Two-Tone Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 120 mA, I_{DQ2} = 90 mA, P_{out} = 5 W Avg., 1805-1880 MHz					
Power Gain	G_{ps}	—	29	—	dB
Power Added Efficiency	PAE	—	29	—	%
Intermodulation Distortion	IMD	—	-34	—	dBc
Input Return Loss	IRL	—	-15	—	dB
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 105 mA, I_{DQ2} = 95 mA, P_{out} = 3.2 W Avg., 1805-1880 MHz or 1930-1990 MHz EDGE Modulation					
Power Gain	G_{ps}	—	29	—	dB
Error Vector Magnitude	EVM	—	1.1	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-67	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-76	—	dBc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 5. Electrical Characteristics — continued (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical CW Performances (In Freescale CW Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 120 mA, I_{DQ2} = 90 mA, P_{out} = 2.25 W Avg., 1805-1990 MHz					
Power Gain	G_{ps}	—	29	—	dB
Power Added Efficiency	PAE	—	19	—	%
Input Return Loss	IRL	—	-13	—	dB



Z1	0.120″ x 0.044″ Microstrip	Z7	0.917″ x 0.050″ Microstrip
Z2	0.257″ x 0.044″ Microstrip	Z8	0.304″ x 0.050″ Microstrip
Z3	0.103″ x 0.170″ Microstrip	Z9	0.710″ x 0.050″ Microstrip
Z4	0.195″ x 0.122″ Microstrip	Z10	1.296″ x 0.400″ Microstrip
Z5	0.388″ x 0.084″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.50
Z6	0.273″ x 0.044″ Microstrip		

Figure 3. MHV5IC1810NR2 Test Circuit Schematic — 1930-1990 MHz

Table 6. MHV5IC1810NR2 Test Circuit Component Designations and Values — 1930-1990 MHz

Part	Description	Part Number	Manufacturer
C2	22 pF 100A Chip Capacitor	100A220GWT	ATC
C3, C4, C5, C6	8.2 pF 100A Chip Capacitors	100A8R2CW	ATC
C7, C8, C9	10 nF Chip Capacitors (0805)	08055C103KAT	AVX
C10, C11	6.8 μF Chip Capacitors (1812)	C4532X5R1H685MT	TDK
C12, C13	3.3 pF 100A Chip Capacitors	100A3R3BW	ATC
C14, C15	0.5 pF 100A Chip Capacitors	100A0R5BW	ATC
R1, R2	1 kΩ, 1/8 W Chip Resistors (0805)		

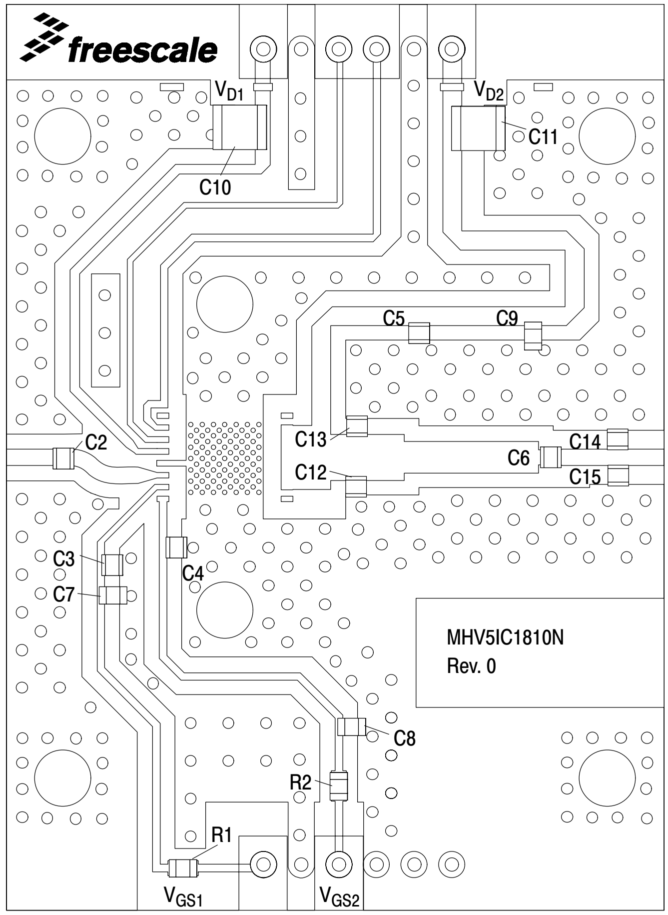


Figure 4. MHV5IC1810NR2 Test Circuit Component Layout — 1930-1990 MHz

TYPICAL CHARACTERISTICS — 1930-1990 MHz

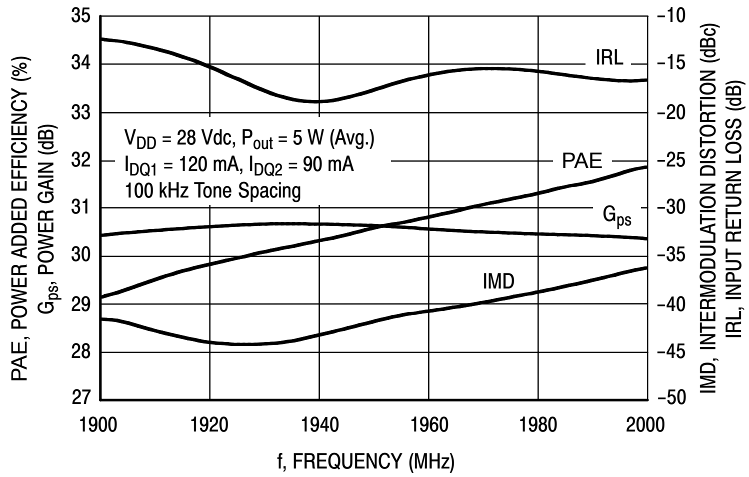


Figure 5. Two-Tone Wideband Performance @ P_{out} = 5 Watts (Avg.)

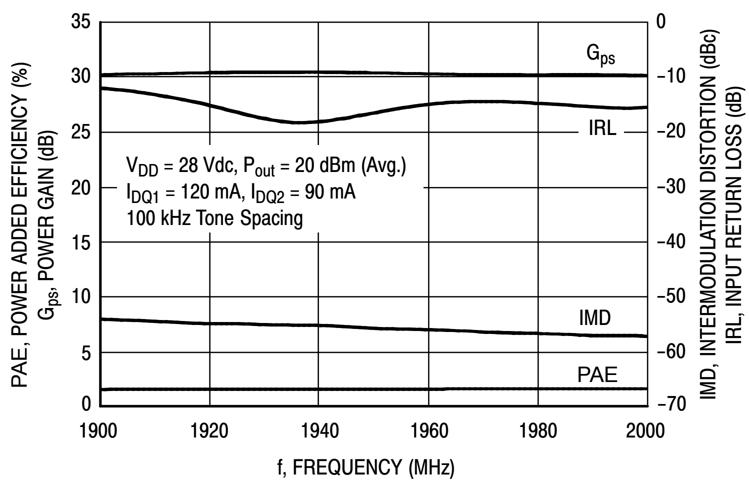


Figure 6. Two-Tone Wideband Performance @ P_{out} = 20 dBm (Avg.)

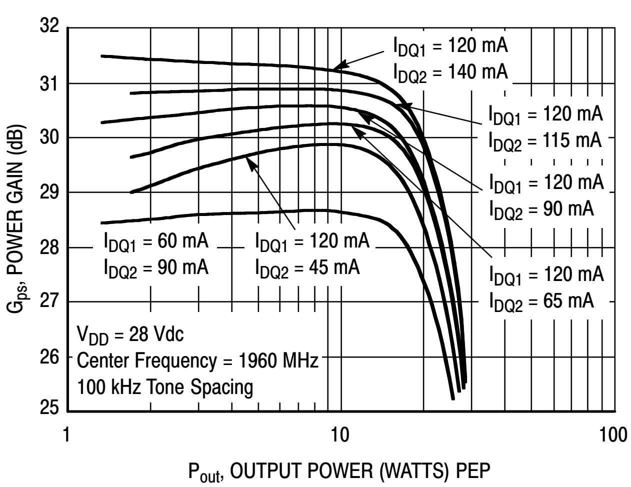


Figure 7. Two-Tone Power Gain versus Output Power

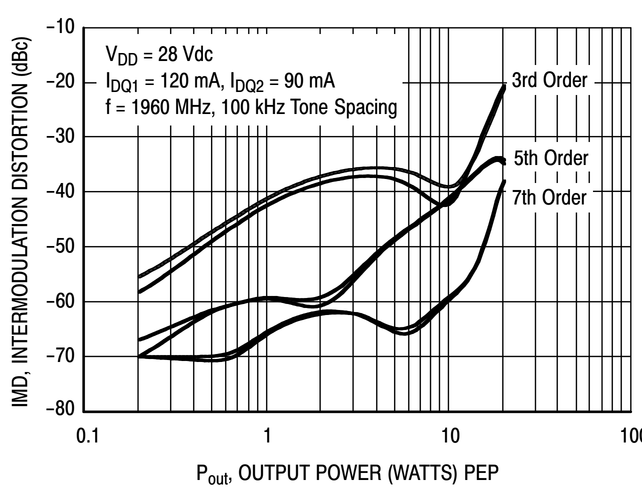


Figure 8. Intermodulation Distortion Products versus Output Power

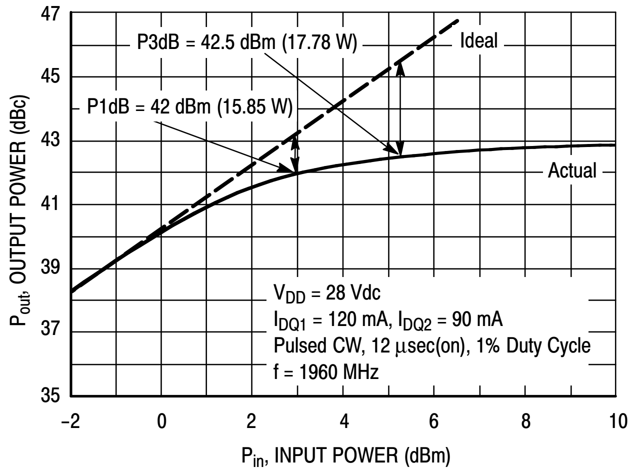


Figure 9. Pulse CW Output Power versus Input Power

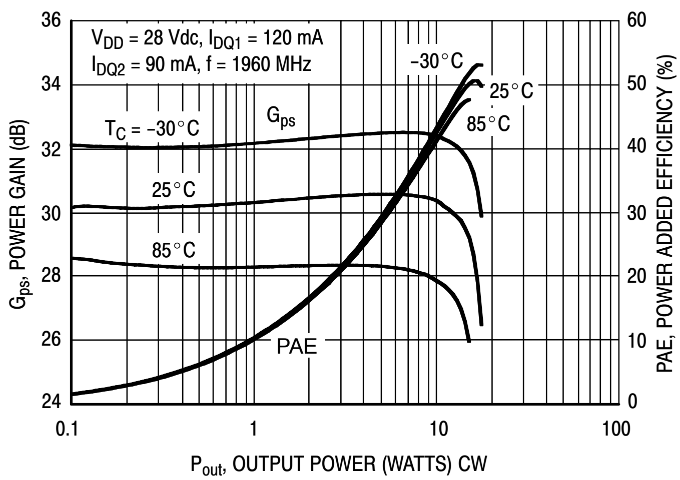


Figure 10. Power Gain and Power Added Efficiency versus CW Output Power

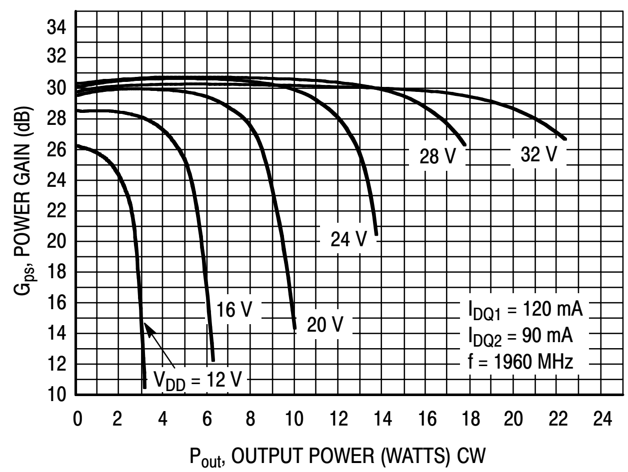


Figure 11. Power Gain versus Output Power

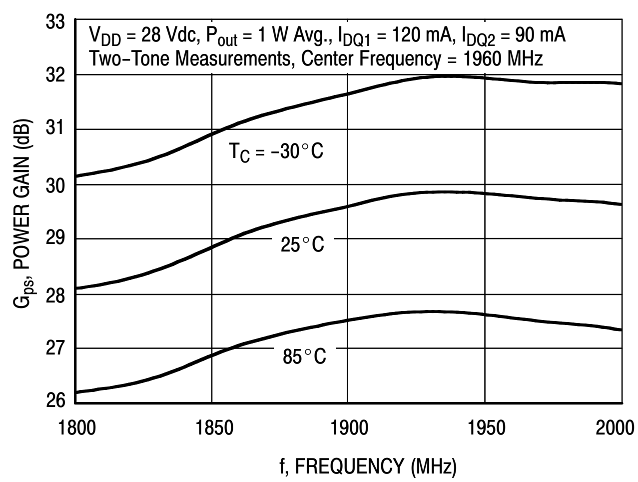


Figure 12. Power Gain versus Frequency

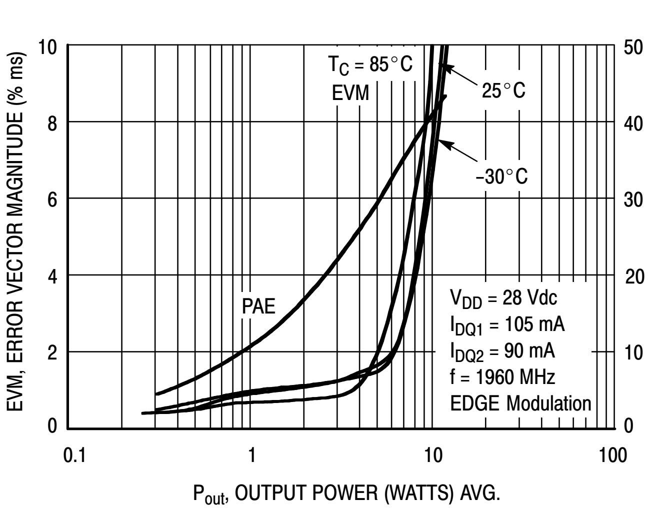


Figure 13. EVM and Power Added Efficiency versus Output Power

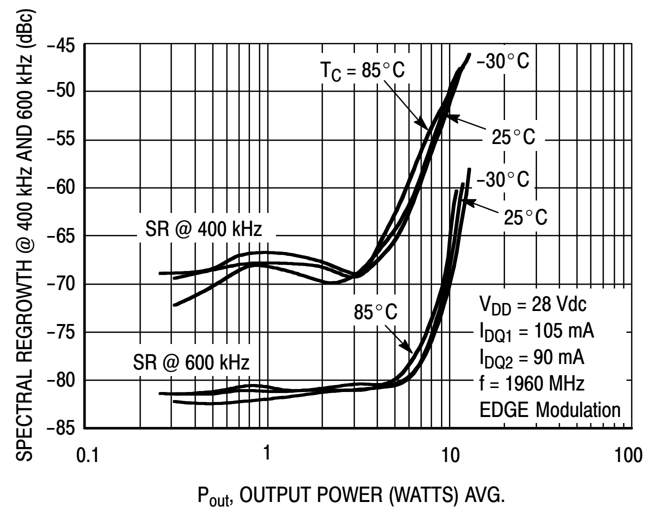
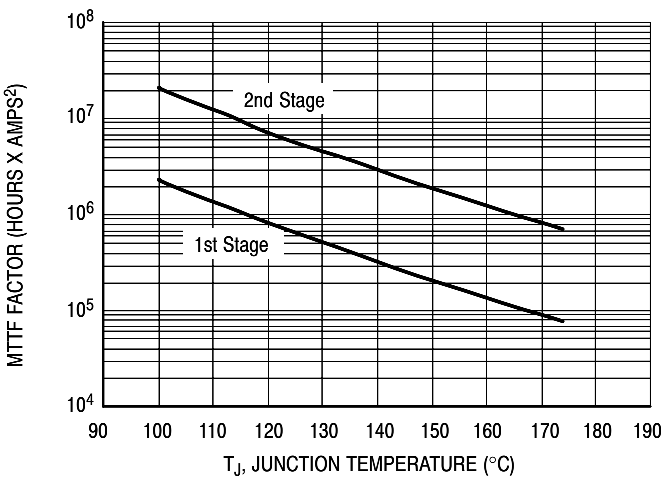


Figure 14. Spectral Regrowth at 400 and 600 kHz versus Output Power



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 15. MTTF Factor versus Junction Temperature

GSM TEST SIGNAL

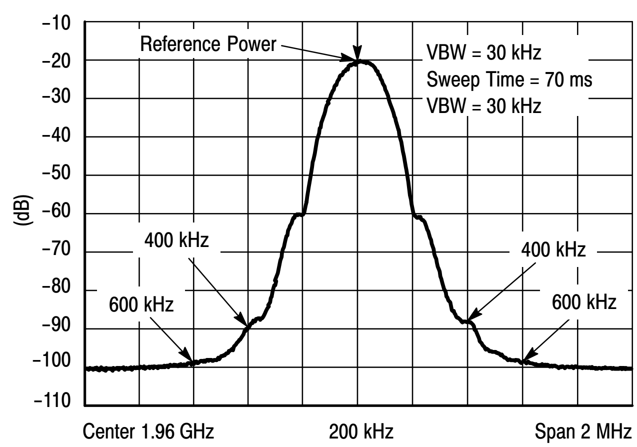
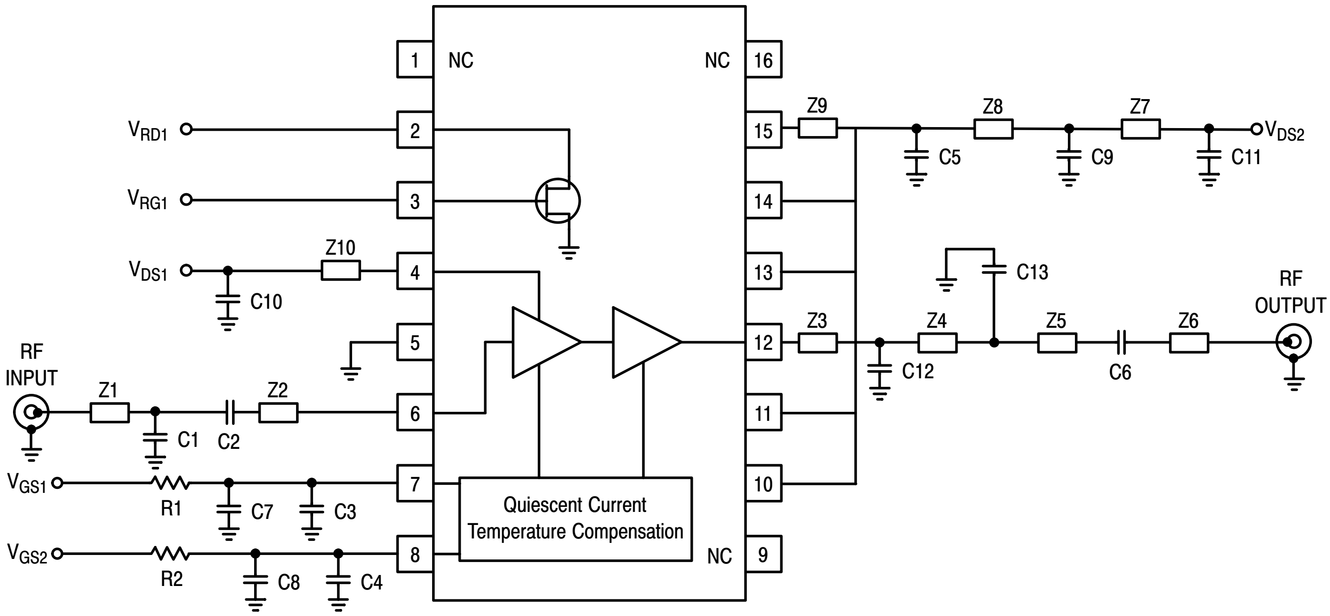


Figure 16. EDGE Spectrum



Z1	0.120″ x 0.044″ Microstrip	Z7	0.917″ x 0.050″ Microstrip
Z2	0.257″ x 0.044″ Microstrip	Z8	0.304″ x 0.050″ Microstrip
Z3	0.274″ x 0.170″ Microstrip	Z9	0.710″ x 0.050″ Microstrip
Z4	0.112″ x 0.084″ Microstrip	Z10	1.296″ x 0.400″ Microstrip
Z5	0.289″ x 0.084″ Microstrip	PCB	Rogers 4350, 0.020″, ε_r = 3.50
Z6	0.273″ x 0.044″ Microstrip		

Figure 17. MHV5IC1810NR2 Test Circuit Schematic — 1805-1880 MHz

Table 7. MHV5IC1810NR2 Test Circuit Component Designations and Values — 1805-1880 MHz

Part	Description	Part Number	Manufacturer
C1	0.8 pF 100A Chip Capacitor	100A0R8BW	ATC
C2	27 pF 100A Chip Capacitor	100A270GWT	ATC
C3, C4, C5, C6	8.2 pF 100A Chip Capacitors	100A8R2CW	ATC
C7, C8, C9	10 nF Chip Capacitors (0805)	08055C103KAT	AVX
C10, C11	6.8 μF Chip Capacitors (1812)	C4532X5R1H685MT	TDK
C12, C13	3.3 pF 100A Chip Capacitors	100A3R3BW	ATC
R1, R2	1 kΩ, 1/8 W Chip Resistors (0805)		

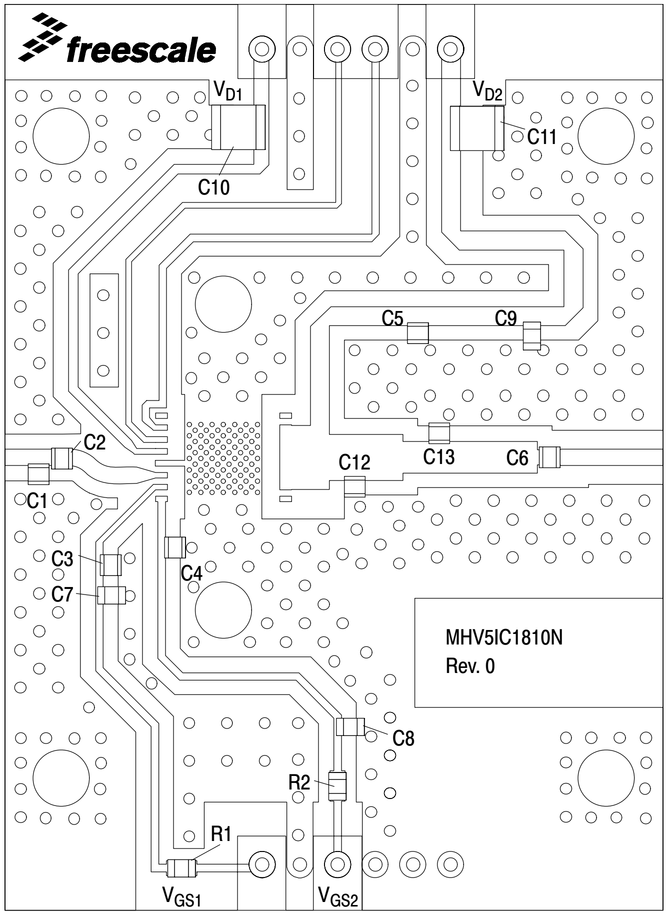


Figure 18. MHV5IC1810NR2 Test Circuit Component Layout — 1805-1880 MHz

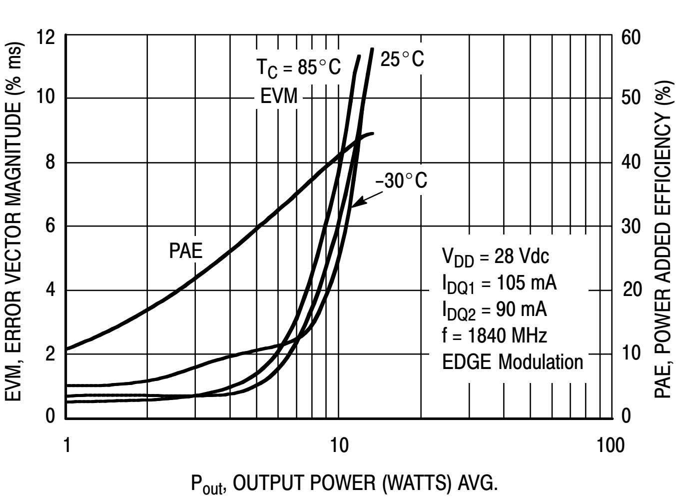


Figure 19. Spectral Regrowth at 400 and 600 kHz versus Output Power

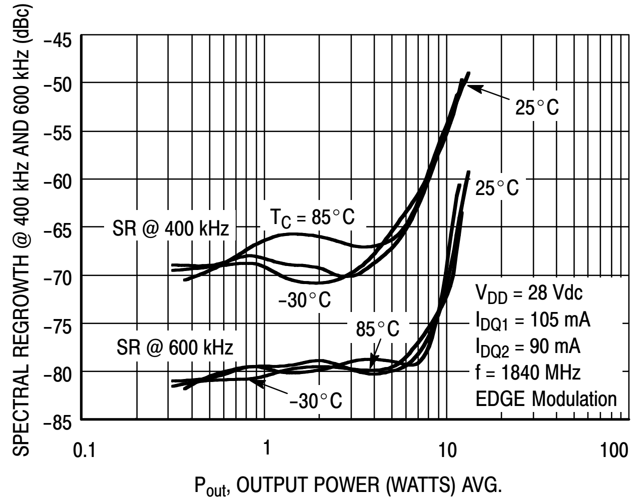
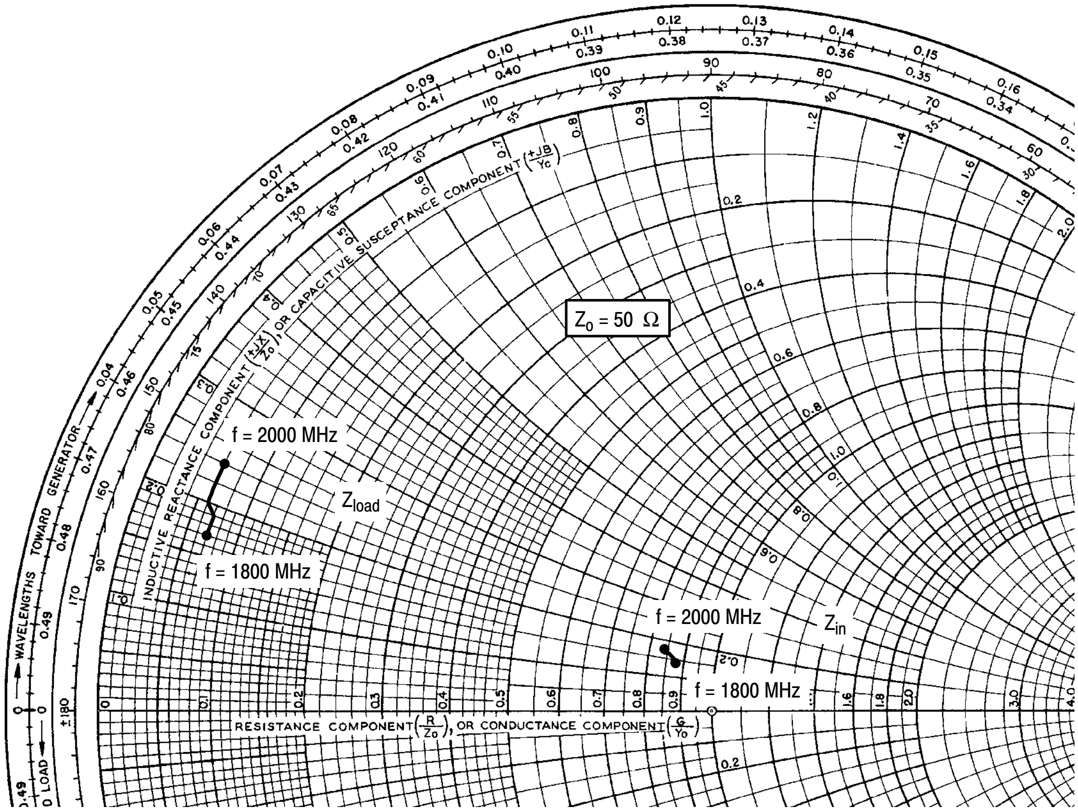


Figure 20. Spectral Regrowth at 400 and 600 kHz versus Output Power



V_{DD} = 28 Vdc, I_{DQ1} = 120 mA, I_{DQ2} = 90 mA, P_{out} = 5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
1800	43.82 + j6.83	3.49 + j8.58
1820	43.67 + j7.10	3.43 + j8.96
1840	43.50 + j7.34	3.36 + j9.33
1860	43.31 + j7.55	3.31 + j9.68
1880	43.13 + j7.76	3.24 + j10.04
1900	42.96 + j7.96	3.19 + j10.38
1920	42.76 + j8.15	3.14 + j10.72
1940	42.56 + j8.34	3.07 + j11.03
1960	42.36 + j8.50	3.04 + j11.36
1980	42.16 + j8.65	2.99 + j11.65
2000	41.97 + j8.79	2.94 + j11.94

Z_{in} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

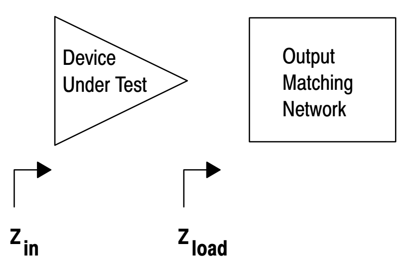
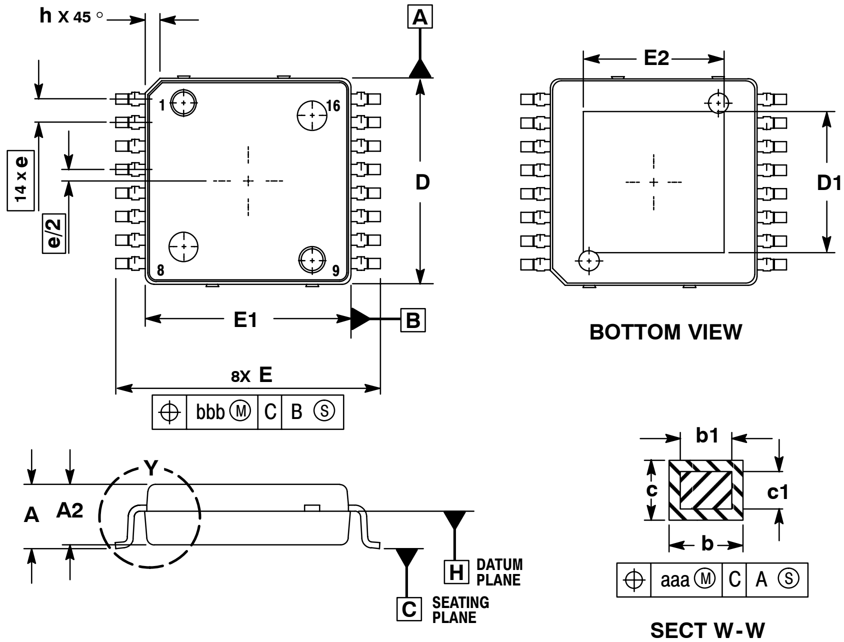


Figure 21. Series Equivalent Input and Load Impedance

NOTES

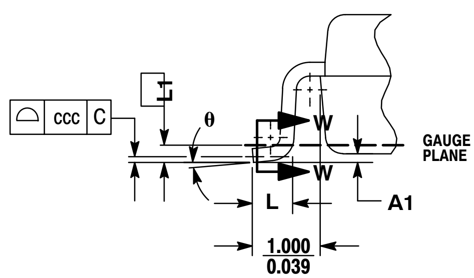
NOTES

PACKAGE DIMENSIONS



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

	MILLIMETERS	
DIM	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	



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